EXHIBIT 2

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC. and SAMSUNG SEMICONDUCTOR, INC., Defendants.	Civil Case No. 2:21-cv-00463-JRG **JURY TRIAL DEMANDED**

DEFENDANTS' IDENTIFICATION OF
CLAIM TERMS REQUIRING CONSTRUCTION

Pursuant to P.R. 4-1 and the Court's Docket Control Order (Dkt. No. 34), Defendants Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc., (collectively, "Defendants") identify the following terms, phrases, and/or clauses of U.S. Patent Nos. 10,860,506 (the "'506 patent"); 10,949,339 (the "'339 patent"); 11,016,918 (the "'918 patent"); 11,232,054 (the "'054 patent"); 8,787,060 (the "'060 patent"); and 9,318,160 (the "'160 patent") (collectively, the "Asserted Patents"), which they contend require construction by the Court.

The claim terms, phases, and/or clauses occur in independent and/or dependent claims of the Asserted Patents. Unless otherwise indicated below, any additional occurrence, including in related asserted patents, of a listed claim term, phrase, and/or clause is intended to receive the same construction as the listed term, phrase, and/or clause, regardless of whether the later occurrence is also listed below.

Defendants reserve the right to modify, supplement, or amend their list of claim terms, phrases, and/or clauses set forth below. Additionally, Defendants reserve the right to separately request construction of portions of the identified claim terms, phrases, and/or clauses.

Defendants further reserve all rights to assert that terms, phrases, and/or clauses in the Asserted Patents are invalid under 35 U.S.C. § 112, including without limitation the terms, phrases, and/or clauses listed in Defendants' P.R. 4-1 disclosure and/or the terms, phrases, and/or clauses listed in Defendants' P.R 3-3 Invalidity Contentions and any supplements thereto.

The inclusion of any claim terms, phrases, and/or clauses on this list is not intended, and should not be construed to mean, that any such terms, phrases, and/or clauses have a special or uncommon meaning. Additionally, the inclusion of any claim terms, phrases, and/or clauses on this list is not intended to and does not constitute an admission that the term, phrase, and/or clause is capable of construction and not indefinite under 35 U.S.C. § 112, lacking enablement or adequate written description, or otherwise incapable of construction. Defendants reserve the right to contest any such terms, phrases, and/or clauses and the validity of any claim of the Asserted Patents.

This list is preliminary and Defendants reserve the right to add, delete, and/or amend claim terms, phrases, and/or clauses from the list based on, without limitation, the list(s) propounded by plaintiff Netlist, Inc. ("Netlist") pursuant to this Local Rule, the conferences called for by the Local Patent Rules, or any information learned throughout the course of discovery. Defendants reserve the right to include Netlist's proposed claim terms, phrases, and/or clauses in their list.

To the extent the claim terms, phrases, and/or clauses set forth herein include particular terms, phrases, and/or clauses appropriate to be construed separately, such terms, phrases, and/or clauses are deemed part of this disclosed list. Similarly, to the extent it is appropriate to construe terms, phrases, and/or clauses listed herein in the context of additional claim language, such additional language is deemed part of this disclosure.

TERMS FOR CONSTRUCTION

	Claim Terms, Phrases, or Clauses for Construction	Claim Number(s)
1	"a second plurality of address and control signals"	'918 patent: 1-3, 5-7, 9-13, 15, 21
2	"dual buck converter" / "dual-buck converter"	'918 patent: 2, 17, 28 '054 patent: 15
3	"configuration information"	'918 patent: 10, 11, 15, 22
4	"writes information"	'918 patent: 11
5	"write operation"	'918 patent: 12, 18, 19, 25, 26
6	"pre-regulated input voltage" / "input voltage"	'918 patent: 16-22, 30
7	"data information"	'918 patent: 19, 26
8	"non-volatile memory"	'918 patent: 10-12, 15, 19, 22, 26 '054 patent: 5, 7, 23, 24
9	"first" / "second" / "third" / "fourth" "regulated voltages" / "voltage amplitude(s)"	'918 patent: All asserted claims
10	"the plurality of SDRAM devices are powered on"	'918 patent: 23-30
11	"operable state"	'054 patent: 4-7, 11-12, 16-17, 23, 25-28
12	"write operation to transfer data"	'054 patent: 5, 7, 23, 24
13	"at least three regulated voltages" / "plurality of regulated voltages"	'054 patent: All asserted claims
14	"array die"	'060 patent: All asserted claims '160 patent: All asserted claims
15	"The memory package of claim 1, wherein a first number of array dies in the first group of array dies and a second number of at least one array die in the second group of at least one array die are selected in consideration of a load of the first die interconnect and a load of the second die interconnect so as to reduce a difference between a first load on the first data conduit and a second load on the second data conduit, the first load including a load of the first die interconnect, and a load of the first group of array dies, and the second load including a load of the second die interconnect and a load of the second group of at least one array die."	'060 patent: 7
16	"The method of claim 20, further comprising: selecting a first driver size for the first driver based, at least in part, on a load on the first driver; and selecting a second driver size for the second driver	'060 patent: 21

	Claim Terms, Phrases, or Clauses for Construction	Claim Number(s)
	based, at least in part, on a load on the second driver."	
17	"control die"	'060 patent: All asserted claims '160 patent: All asserted claims
18	"a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals."	'060 patent: 1-10
19	" a control die comprising at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, at least a second data conduit between the second die interconnect and the first terminal, and chip select conduits for providing chip select signals to respective array dies"	'060 patent: 11-14, 16-19
20	" providing chip select signals to respective array dies through the control die, the chip select signals being related to at least some of the control signals; and selecting one of a first driver and a second driver in the control die to drive the data signal via a corresponding one of the first die interconnect and the second die interconnect to an array die selected by at least one of the chip select signals, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies.	'060 patent: 20-21, 23-28
21	"a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first drivers each having a first	'160 patent: All asserted claims

	Claim Terms, Phrases, or Clauses for Construction	Claim Number(s)
	driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size."	
22	"previous operations"	'506 patent: 1-3, 11, 15, 16
23	"before receiving the input C/A signals corresponding to the memory read operation"	'506 patent: 14
24	"each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals"	'339 patent: 1
25	"the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period"	'339 patent: 1
26	"logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period"	'339 patent: 1
27	"each respective data transmission circuit is configurable to enable the data paths for a first time period in accordance with a latency parameter to actively drive a respective section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period"	'339 patent: 11
28	"the respective data transmission circuit in response to the module control signals is configured to enable a first subset of the first tristate buffers to drive the first subsection of the respective section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks, and to enable a second subset of the first tristate buffers to drive a second subsection of the respective section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one	'339 patent: 11

	Claim Terms, Phrases, or Clauses for Construction	Claim Number(s)
	of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit-wide ranks"	
29	"each respective buffer further includes logic configurable to enable the data paths for a first time period to actively drive a respective section of the first N-bit wide data associated with the first memory operation from the second side to the first side during the first time period, and to enable the data paths for a second time period subsequent to the first time period to actively drive a respective section of the second N-bit wide data associated with the second memory operation from the second side to the first side during the second time period"	'339 patent: 19
30	"each respective n-bit-wide data buffer includes … a first set of tristate buffers configurable to drive the respective n-bit section of the write data to the respective module data lines, … a second set of tristate buffers configurable to drive the respective n-bit section of the read data to the respective set of data signal lines, and logic configurable to control at least the first set of tristate buffers and the second set of tristate buffers"	'339 patent: 27
31	"a module controller . . . configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals"	'339 patent: 1
32	"a module controller . . . configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank among the multiple N-bit-wide ranks,	'339 patent: 11

	Claim Terms, Phrases, or Clauses for Construction	Claim Number(s)
	and to output registered address and control signals in response to the input address and control signal, wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to transmit module control signals to the n/2 data transmission circuits in response to the input address and control signals"	
33	"a module controller . . . configurable to receive from the memory controller via the address and control signal lines first address and control signals for a first memory operation to read first N-bit-wide data from a first N-bit-wide rank among the multiple ranks and to subsequently receive second address and control signals for a second memory operation to read second N-bit-wide data from a second N-bit-wide rank among the multiple ranks, the module controller being further configurable to output first registered address and control signals for the first memory operation in response to receiving the first address and control signals and to output second registered address and control signals for the second memory operation in response to receiving the second address and control signals, wherein the first registered address and control signals cause the first N-bit-wide rank to output the first N-bit-wide data associated with the first memory operation, and the second registered address and control signals cause the second N-bit-wide rank to output the second N-bit-wide data associated with the second memory operation, wherein the module controller is further configurable to output first module control signals for the first memory operation in response to receiving the first address and control signals and to output second module control signals for the second memory operation in response to receiving the second address and control signals"	'339 patent: 19
34	"a module controller . . . configurable to receive from the memory controller via the address and control signal lines first address and control signals for a memory write operation and to subsequently receive second address and control signals for a memory read operation, the module controller being	'339 patent: 27

	Claim Terms, Phrases, or Clauses for Construction	Claim Number(s)
	further configurable to output first registered address and control signals and first module control signals for the memory write operation in response to the first address and control signals, and to output second registered address and control signals and second module control signals for the memory read operation in response to the second address and control signals"	

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CERTIFICATE OF SERVICE

I certify that on July 22, 2022 a true and correct copy of the foregoing was served on counsel of record for Plaintiff via electronic mail.

/s/ *Tony Nguyen*
Tony Nguyen